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IR-1698 (2-2027)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of:

Daniel M. Kinzer, et al.

Date: September 2, 2003

Serial No.: 09/891,727

Group Art Unit: 2822

Filed: June 26, 2001

For: LATERAL SUPERJUNCTION SEMICONDUCTOR DEVICE

13 # / Appeal Brief

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. §1.192

9/13/03

Sir:

This appeal is taken from the Examiner's final rejection dated January 28, 2003, in connection with the above-identified application. The Notice of Appeal was filed in the United States Patent and Trademark Office on June 30, 2003.

I. Status of Claims

Claims 1-28 stand rejected and are pending on appeal.

II. Real Party in Interest

The real party in interest is the assignee, International Rectifier Corporation.

III. Related Appeals and Interferences

The applicants, the assignee and the undersigned attorneys are not aware of any related appeals or interferences.

IV. Status of Amendments

An Amendment/Submission containing arguments regarding the patentability of the claims was filed after the final rejection on May 27, 2003, and was entered for the purposes of appeal.

V. Summary of Invention

Planar, lateral conduction type MOSgated devices such as planar MOSFETs, include on a common major surface of a semiconductive body, a drain region, a source region and a channel region. The channel region can be inverted by a MOSgated structure to form a channel which allows the source region and the drain region to become electrically connected.

The present invention relates to planar, lateral conduction type MOSgated devices. A device according to the present invention would include a plurality of trenches disposed between a drain region and a MOSgate structure of the device. Specifically, the trenches are positioned such that the mesas, which are created by the trenches, extend between the drain and the MOSgate structure.

According to the present invention, the mesas are doped with dopants of one conductivity and include diffusions of another conductivity on their sidewalls. The thickness of the mesas and the concentration of the dopants in the mesas and the diffusions in the sidewalls of the trenches are selected such that under a reverse voltage, the diffusion on the sidewalls of the trenches and the mesas fully deplete one another. This feature significantly improves the ability of the device to withstand breakdown under reverse voltage conditions.

Figs. 4, 5, and 6 (reproduced below) show the preferred embodiment of a device according to the present invention.

FIG. 4

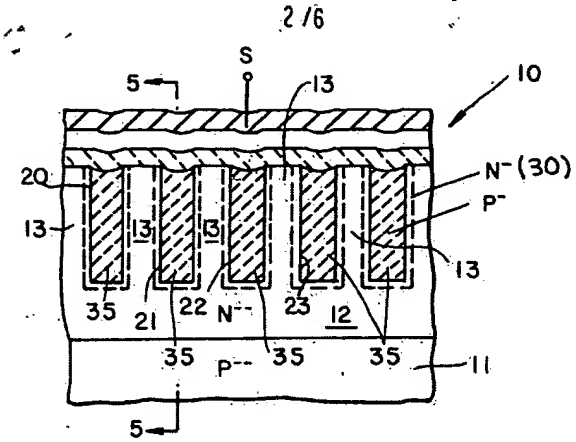


FIG. 6

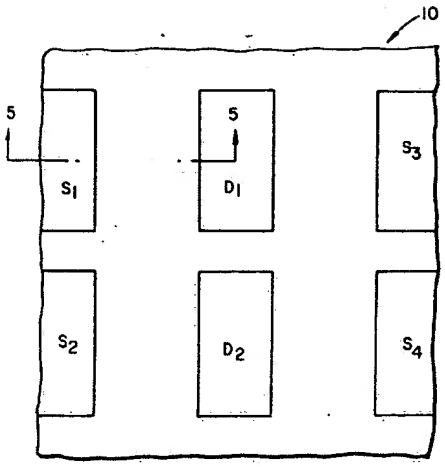


FIG. 5

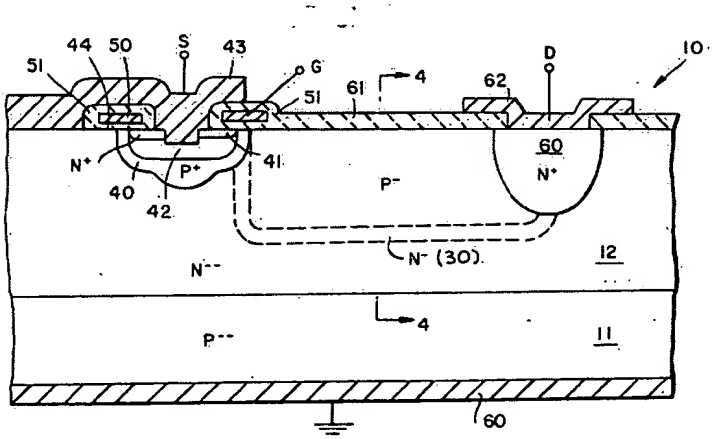


Fig. 5 shows the cross-section of the preferred embodiment along line 5-5 (Figs. 4 and 6), looking in the direction of the arrows. As is quite clear from Fig. 5, a number of trenches 20-23 (and consequently the mesas adjacent to the trenches) extend between the drain region 60 and the MOSgate structure of the device.

As shown by Fig. 4, the mesas are doped with P type dopants while the walls of the trenches 20-23 adjacent to the mesas are doped with N type dopants. It should be noted that the drain region 60 is also doped with N type dopants, which is the same as the dopants forming the diffusions in the sidewalls of the trenches.

The MOSgate structure includes gate electrode (marked G) which is disposed over the gate oxide. The gate oxide is disposed over the channel region which is adjacent a source region 41. When the channel region is inverted (to N conductivity) by application of a voltage to the gate electrode, a channel is formed to connect the source region 41 to the drain region 60 through the diffusions 30 in the sidewalls of the trenches/mesas. The thickness of the mesas and the concentration of dopants in the mesas and the diffusions 30 are selected such that under a reverse bias conditions the two regions deplete completely.

Claim 1 calls for:

1. A lateral conductive superjunction semiconductor device comprising: a trench receiving layer (13) of one of the conductivity types supported atop a substrate (11) and having an upper surface; a plurality of spaced laterally extending trenches (20-23) formed into said trench-receiving layer (13); a diffusion of the other of said conductivity types (30) extending into the walls of said trenches (20-23) and having a given depth and a given concentration; said trenches defining mesas between them of a given width and a given concentration; a drain region (60) of said other of said conductivity types extending into said trench receiving layer (13) and disposed at one end of said mesas; a MOSgate structure including a source region (41), base region (42) and a gate electrode (50) disposed at the other end of said mesas; the thickness and concentration of said mesas and said diffusions being selected to cause each to fully deplete under blocking voltage conditions, wherein each of said mesas extends between said drain region and said MOSgate structure.

Numerals have been included to indicate the corresponding features in the preferred embodiment.

VI. Issues on Appeal

1. Whether claim 1 is obvious over U.S. Patent No. 5,844,275 (Kitamura et al.) in view of U.S. Patent No. 5,861,675 (Ranjan) in further view of U.S. Patent No. 6,040,600 (Uenishi et al.).

VII. Grouping of Claims

Claims 1-28 stand or fall together.

VIII. Argument

Claim 1 is the only independent claim in the application. The remaining claims 2-28 depend from claim 1. Consequently, claims 2-28 should be allowable if claim 1 is allowed.

Claim 1 has been rejected under 35 U.S.C. §103(a) over Kitamura et al. in view of Ranjan, Sakakibara et al. U.S. Patent No. 5,449,946, and Uenishi et al.

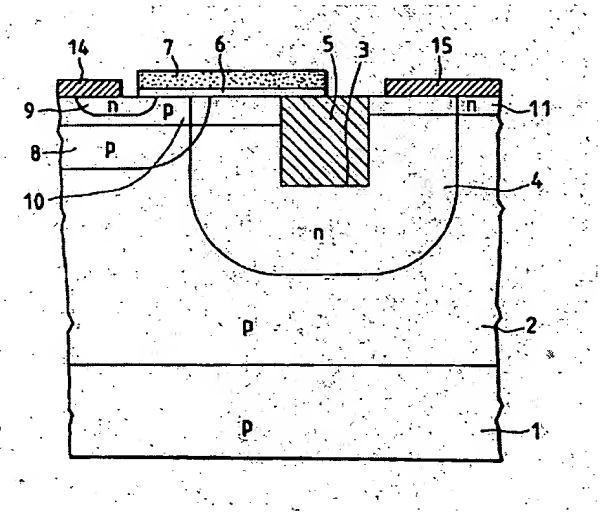
In the amendment filed on May 27, 2003, claim 1 was amended to avoid Sakakibara. The amendment was entered for the purposes of this appeal. Thus, Sakakibara et al. will not be discussed further.

The Examiner has stated that Kitamura et al. show all of the features of claim 1 except for "the thickness and concentration of said mesas and said diffusions [are] selected to cause each to fully deplete under blocking voltage conditions" as called for by claim 1. It has been set forth, however, that Ranjan at Col. 2, lines 7-16 "discloses a semiconductor device where the mesas and diffusions vary". Thus, the Examiner has asserted that a skilled person would be motivated to modify the device of Kitamura "to include mesas and diffusions that vary as disclosed in

Ranjan because it provides a smaller lateral extent and takes up less chip area." Final Rejection, January 28, 2003, Page 4.

It has also been set forth that Kitamura et al. show all of the features of claim 1 except for "mesas [that] extend between said drain and said MOSgate structure." However, it has been set forth that Figure 1 of Uenishi et al. "discloses a semiconductor device where the mesas extend between said drain and said MOSgate structure". Therefore, the Examiner has asserted that one skilled in the art, based on the disclosure of Uenishi et al., could modify the device shown by Kitamura to include mesas that extend between the drain and the gate structure. According to the Office Action, the motivation for such a modification is to obtain a high breakdown voltage. Final Rejection, January 28, 2003, Page 4.

Referring now to Fig. 1 (reproduced below) of Kitamura et al., the device shown includes a drain 1, a source 9, a base 8, a gate electrode 7 and a gate oxide 6 forming a gate structure, a single trench 3 surrounded by a drift region 4 of the same conductivity as the drain 11. Fig. 9 shows a plurality of trenches.



As admitted by the Examiner mesas created by the trenches of the device of Kitamura et al. do not extend between the drain and the gate structures. To remedy this deficiency in the prior art the Examiner has cited Fig. 1 of Uenishi et al. Specifically, the Examiner states that

"Uenishi discloses a mesa as defined by Applicant in claim 1 (for example, see Fig. 1) and the motivation to combine in order to provide a high breakdown voltage is disclosed (For example: See Abstract and Column 4 lines 45-50)." See Advisory Action, January 26, 2003.

The Abstract of Uenishi et al. provides:

> An n type diffusion region and a p type diffusion region are formed in a region sandwiched between trenches arranged at a first main surface of a semiconductor substrate. A p type well is formed in the n– and p-type diffusion regions nearer the first main surface. A source n^+ diffusion region is formed at the first main surface within the p type well. A gate electrode layer is formed opposite to the p type well sandwiched between the n type diffusion region and the source n^+ diffusion region with a gate insulating layer disposed therebetween. The n– and p-type diffusion regions each have an impurity concentration distribution diffused from a sidewall surface of a trench. Thus, a fine, micron-order pn repeat structure can be achieved with sufficient precision and a high breakdown voltage semiconductor device is thus obtained which has superior on-state voltage and breakdown voltage as well as fast switching characteristics.

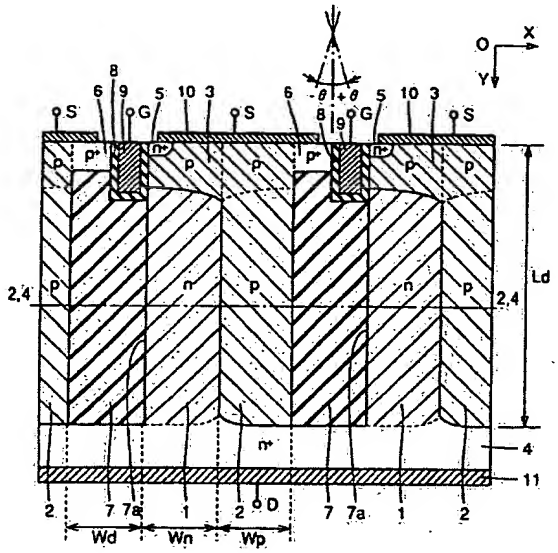
Col. 4, lines 45-50 of Uenishi et al. provides:

> An object of the present invention is to allow a fine pn structure to provide a high breakdown voltage semiconductor device capable of greatly improving the trade-off between the breakdown voltage and on-state voltage thereof.

There is nothing in the cited excerpts from Uenishi et al. that teaches one skilled in the art to place the drain at one end of a plurality of mesas and dispose the gate structure at the other end of a plurality of mesas in order to improve the breakdown voltage characteristics of a planar type MOSgated device.

In addition, no such teaching can be deduced from the teachings of Uenishi et al. Referring to Fig. 1 of Uenishi et al. (reproduced below), the only mesas seen are those created by trenches on the top surface of the device which receive gate structures (marked G). Fig. 1 shows source contacts on the mesas (marked S), while the drain (marked D) of the device is disposed on the surface opposing the surface that has mesas. Thus, the mesas run above and parallel to the

drain. The drain does not reside at one end of the mesas. Uenishi et al., therefore, do not show or even suggest mesas that extend "between said drain region and said MOSgate structure", contrary to the Examiner's assertion.



As also admitted by the Examiner, Kitamura et al. do not show diffusions of a second conductivity type (opposite to the conductivity of the trench receiving layer) "extending into the walls of said trenches."

The Examiner, however, asserts that one skilled in the art would be motivated to form such diffusions into the sidewalls of the trenches shown by Kitamura et al. based on the teachings of Ranjan.

It should first be noted that claim 1 calls for diffusions of the other conductivity type (opposite to the conductivity of the trench receiving layer). Claim 1 also calls for the drain to have the same conductivity (other conductivity) as the diffusions. If in fact the device of Kitamura et al. is modified to include diffusions of a conductivity opposite to the trench receiving layer (which is N-type), it will have diffusions of an opposite conductivity (P-type). Such a diffusion will necessarily have a conductivity opposite to the drain region. Thus, even if Kitamura et al. is modified to have diffusions of opposite conductivity to the conductivity of the trench receiving layer, the resulting device will not include the subject matter of claim 1, which

calls for the conductivity of the drain and the diffusions in the sidewalls of the trenches to be the same.

As motivation for modifying the device shown by Kitamura et al. the Examiner states that Ranjan teaches varying mesas and diffusions result in "smaller lateral extent and takes up less chip area." The Examiner has cited Col. 2, lines 7-16 for support:

> In the resulting structure, a variation of the depth of top (diffused) resurf region will have a much smaller effect on the charge contained within the pinched region beneath it. This results in a better control over breakdown voltage with a much thinner epitaxial layer for a given breakdown voltage. The thinner epitaxial layer, in turn, reduces the diffusion processing time needed for forming isolation diffusions and the isolation diffusions have a smaller lateral extent and take up less chip area.

The semiconductor device shown by Ranjan does not show any mesas. Thus, it can't be said that somehow it teaches that the thickness and concentration of mesas and diffusions can be varied to "to fully deplete under blocking voltage conditions".

Furthermore, in the cited excerpt, Ranjan teaches that if the epitaxial layer (the layer in which the device is formed) is made thinner it takes less time to form isolation diffusions 23, which must extend from the top of the epitaxial layer to the substrate 11 below to function properly. As is well known in the art, when diffusion is used to form a conductive region in a semiconductive body, the lateral width of the diffused region grows as the region is diffused deeper because dopants diffuse into the semiconductive body in all directions. All Ranjan is stating is that if the epitaxial layer in which isolation diffusions 23 are formed is thinner, the isolation diffusions 23 will not have to be as deep, and thus less lateral space will be occupied by the isolation diffusions 23.

The Examiner has not clearly explained how, based on the cited excerpt, one skilled in the art could devise a structure in which the diffusions in the sidewalls of the mesas and the mesas would fully deplete under a reverse voltage. Teaching that varying thicknesses and concentrations of different regions in a semiconductor device can vary the behavior of the device is simply too vague a teaching to lead a skilled person in the art to select the concentration of the

diffusions in the sidewalls of the mesas and the thickness of the mesas so that the two regions fully deplete under a reverse voltage.

In response to the citing of Ranjan, it was argued to the Examiner that Ranjan does not set forth having diffusions selected to fully deplete under a reverse voltage.

The Examiner in response cited col. 1, lines 16-21 of Ranjan (See Advisory Action):

> High voltage semiconductor devices commonly employ a resurf region which is a low concentration region between areas of high potential difference. The resurf region depletes as the voltage difference increases, and is fully depleted before the maximum voltage difference is applied.

The cited excerpt again discloses generalities about diffusion concentrations in other devices. Specifically, it states that when resurf concentrations are used in certain applications, the resurf region fully depletes before the maximum voltage is reached. There is nothing in that excerpt that teaches that two regions fully deplete one another under reverse voltage. To be more specific, nothing in the cited excerpt teaches or suggests selecting the concentration of the diffusion and the thickness of a mesa in which the diffusion is formed such that the two regions fully deplete under a reverse voltage, as called for by claim 1.

It is respectfully submitted that a prima facie case of obviousness has not been established to reject claim 1. Reversal of the rejection is requested.

IX. Conclusion

Claim 1 is not obvious over Kitamura et al. in view of Ranjan and in further view of Uenishi et al. Thus, claim 1 should be allowed.

Claims 2-28 depend from claim 1 and thus should also be allowed.

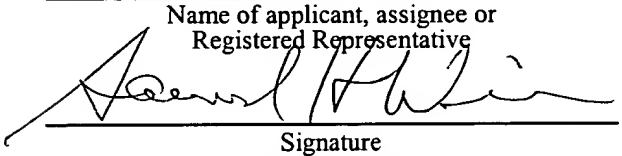
Our check No. 12494, which includes the amount of $320 to cover the appeal brief is attached hereto. This brief is being submitted in triplicate in accordance with 37 C.F.R. 1.192 and applicant reserves the right to request an oral hearing upon receipt of the Examiner's Answer.

If this communication is being filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing the required papers by the number of months which will avoid abandonment under 37 C.F.R §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 2, 2003

Samuel H. Weiner

Name of applicant, assignee or Registered Representative

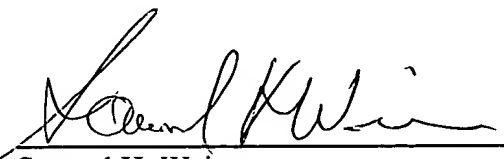


Signature

September 2, 2003

Date of Signature

Respectfully submitted,



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APPENDIX OF CLAIMS ON APPEAL

1. A lateral conductive superjunction semiconductor device comprising: a trench receiving layer of one of the conductivity types supported atop a substrate and having an upper surface; a plurality of spaced laterally extending trenches formed into said trench-receiving layer; a diffusion of the other of said conductivity types extending into the walls of said trenches and having a given depth and a given concentration; said trenches defining mesas between them of a given width and a given concentration; a drain region of said other of said conductivity types extending into said trench receiving layer and disposed at one end of said mesas; a MOSgate structure including a source region, base region and a gate electrode disposed at the other end of said mesas; the thickness and concentration of said mesas and said diffusions being selected to cause each to fully deplete under blocking voltage conditions, wherein each of said mesas extends between said drain region and said MOSgate structure.

2. The device of claim 1 which further includes a dielectric filler in each of said trenches.

3. The device of claim 1 which further includes source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively.

4. The device of claim 1 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

5. The device of claim 1 which includes a further region of said other conductivity interposed between said substrate and said trench- receiving layer; said further region being more lightly doped than said diffusion; said diffusion extending into said further region along the bottoms of said trenches.

6. The device of claim 1 wherein said diffusion extends into said substrate at the bottoms of said trenches.

7. The device of claim 1 which further includes an insulation layer interposed between said substrate and said trench- receiving layer; the upper surface of said insulation layer being coplanar with the bottoms of said trenches.

8. The device of claim 5 which further includes a dielectric filler in each of said trenches.

9. The device of claim 5 which further includes source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively.

10. The device of claim 5 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

11. The device of claim 8 which further includes source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively.

12. The device of claim 8 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

13. The device of claim 9 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

14. The device of claim 11 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

15. The device of claim 6 which further includes a dielectric filler in each of said trenches.

16. The device of claim 6 which further includes source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively.

17. The device of claim 6 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

18. The device of claim 15 which further includes source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively.

19. The device of claim 15 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

20. The device of claim 16 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

21. The device of claim 18 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

22. The device of claim 7 which further includes a dielectric filler in each of said trenches.

23. The device of claim 7 which further includes source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively.

24. The device of claim 7 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

25. The device of claim 22 which further includes source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively.

26. The device of claim 22 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

27. The device of claim 23 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.

28. The device of claim 25 wherein said substrate is a lightly doped P type material and wherein said diffusion and said mesas have RESURF concentrations.